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ACT-IR8200P

IrDA Compliant Protocol Processor

Preliminary Specification

Jan 14, 2003 Rev.0.2c

ACTiSYS reserves the right to make changes without further notice to any products herein to improve reliability, function or design. ACTiSYS does not assume any liability arising out of the application or use of any product or circuit described herein.

Revision History		
Revision	**Date**	**Comment**
Rev. 0.0	02/28/2002	Draft Preliminary Design Specification for internal review.
Rev. 0.0a	06/10/2002	Draft Preliminary Design Specification for internal review.
Rev. 0.1	06/24/2002	Reviewed by Lichen Wang
Rev. 0.1a	11/29/2002	Reviewed by Lichen Wang
Rev. 0.2	12/20/2002	Add implementation information.
Rev. 0.2a	12/31/2002	Modify IrDA port baud rate and flow control for each firmware
Rev. 0.2b	01/13/2003	Modify host baud rate for each firmware.
Rev. 0.2c	01/14/2003	Revise typo. Add notes at IrOBEX transport.

Table of Contents

1. Introduction

The ACT-IR8200P is a low cost, high-integration and Field Programmable microprocessor with on-chip IrDA protocol stack and on-chip Infrared physical encoder/decoder. It offers Infrared communication capability to devices, makes the devices an IrDA- compatible product. In addition, it also offers the following unused functions for customer to utilize:

a) on-chip 12 bit ADC with 8 I/O pins useful for embedded control applications,

b) on-chip USART supports full duplex asynchronous serial communication and 3-wire or 4-wire synchronous peripheral interface (SPI),

c) on-chip 16-bit timer with 3 channels of versatile compare/capture blocks,

d) low power standby with automatic wake-up from IR.

A ready IrDA-compatible internal PCB with RS232 or TTL-level SCI interface is available.

Type \ Part NO / Item		IR8200P-P (1.8V~3.6V)	IR8200P-C (1.8V~3.6V)	IR8200P-B (1.8V~3.6V)
Host Interface	DB-9P RS232 interface	✓	✓	✓
	RS232 Speed (bps)	9.6k	9.6k	9.6k
	CTS/RTS flow control	✓	✓	✓
	DataSize	128 bytes FIFO	128 bytes FIFO	128 bytes FIFO
	Ignore CTS/DSR	✓	✓	✓
	None, 8, 1	✓	✓	✓
IrDA Protocol Stack	IrDA Secondary mode	✓	✓	✓
	IrDA Speed (bps)	9.6k~115.2k	9.6k~57.6k	9.6k~57.6k
	Max. PacketSize	128 bytes	64 bytes	64 bytes
	IrPHY	✓	✓	✓
	IrLAP	✓	✓	✓
	IrLMP	✓	✓	✓
	IrLPT	✓		
	TinyTP		✓	✓
	IrCOMM 9wire cooked		✓	
	IrCOMM 3wire raw	✓		
	IrOBEX Transport			✓
IC	IC Package	QFP 64 pin	QFP 64 pin	QFP 64 pin
	Application	Printer		

2. Features

- Implements IrDA protocol layers
  - IrLAP,
  - IrLMP,
  - IAS,

  optional implementation of
  - TinyTP,
  - IrLPT ,
  - IrOBEX transport.

  And many others with on-chip flash EEPROM firmware.
- Supports serial on-board in-system programming for firmware update and/or customization.
- Includes IrPHY encoding/decoding and interfaces directly to Infrared transceivers for data rate up to 115.2 kbit/s for -ACT-IR8200P-P
  9.6kbit/s,
  19.2kbit/s,
  38.4kbit/s,
  57.6kbit/s,
  115.2kbit/s

  and up to 57.6kbit/s for
  -ACT-IR8200P-C
  9.6kbit/s,
  19.2kbit/s,
  38.4kbit/s,
  57.6kbit/s,

  and up to 57.6kbit/s for
  -ACT-IR8200P-B
  9.6kbit/s,
  19.2kbit/s,
  38.4kbit/s,
  57.6kbit/s,

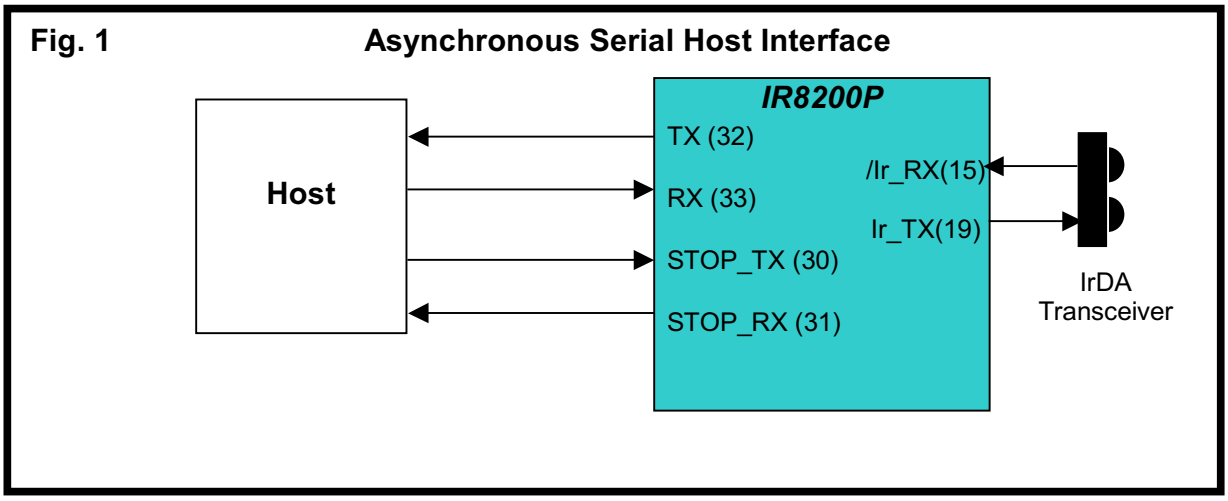
  Only an external Infrared transceiver is needed to complete an IrDA compliant infrared communication subsystem.
- IrDA secondary mode supports.
- Host baud rate supports from 9.6kbit/s to 115.2kbit/s, depends on firmware.
- Both Infrared port and host interface buffer are 128 bytes.
- Low supply voltage, 2.7 V to 3.6 V.
- Low current consumption, 2 uA standby, 3 mA active, 50mA max.
- Small low profile plastic 64-pin QFP package.
- When this chip is used by a host embedded system, the host interface can be:
  - Full duplex asynchronous serial interface (default),
  - 3-wire or 4-wire synchronous peripheral interface (optional),
  - 8-bit or 16-bit parallel interface (optional),
  - Other methods as needed (optional).
- Abundant uncommitted on-chip resources can be utilized to implement a small complete embedded system by itself without a host CPU.
  - 46 uncommitted digital I/O pins
  - 8 of the uncommitted I/O pins can also be -- used by on-chip 12-bit ADC for embedded functions.
  - Uncommitted on-chip USART supports full duplex asynchronous serial communication. It also supports 3-wire or 4-wire synchronous peripheral interface (SPI).
  - Uncommitted on-chip 16-bit timer with 3 channels of versatile compare/capture blocks.
  - Uncommitted 32.768 kHz low power oscillator.
  - Low power standby with wake-up from IR, low power oscillator, and Other sources.

3. Function Description

There are two applicable methods when ACT-IR8200P is used. One is to treat ACT-IR8200P as a component of a host embedded system. Another is as the only processor in a small-embedded system by utilizing the uncommitted on-chip resources with additional firmware.

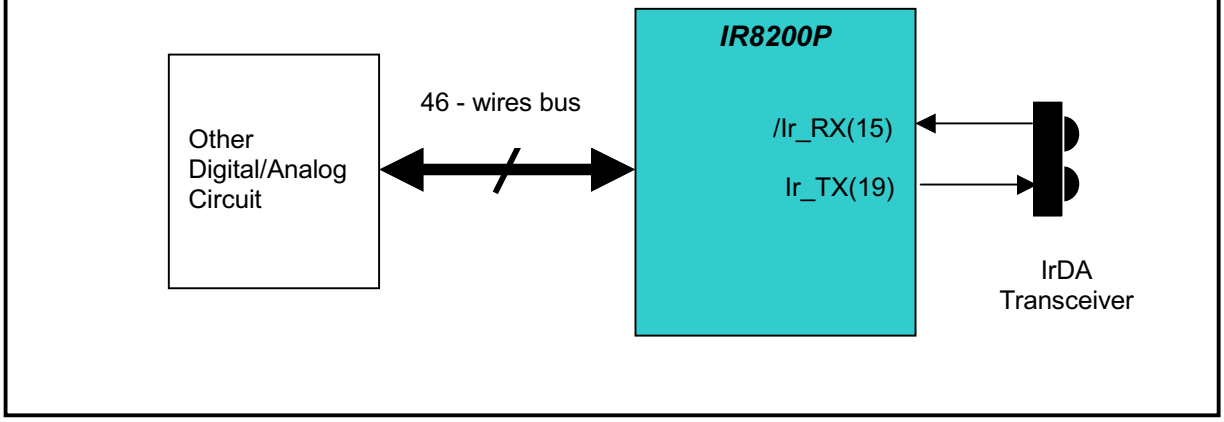
When ACT-IR8200P is used as a component of a host embedded system, the interface can be an asynchronous serial interface with hardware flow-control. SOUT and SIN signals are used for transmit and receive data from host, STOP_TX and STOP_RX signals are used for hardware flow control.
This is shown in Fig. 1.

Fig. 1 Asynchronous Serial Host Interface



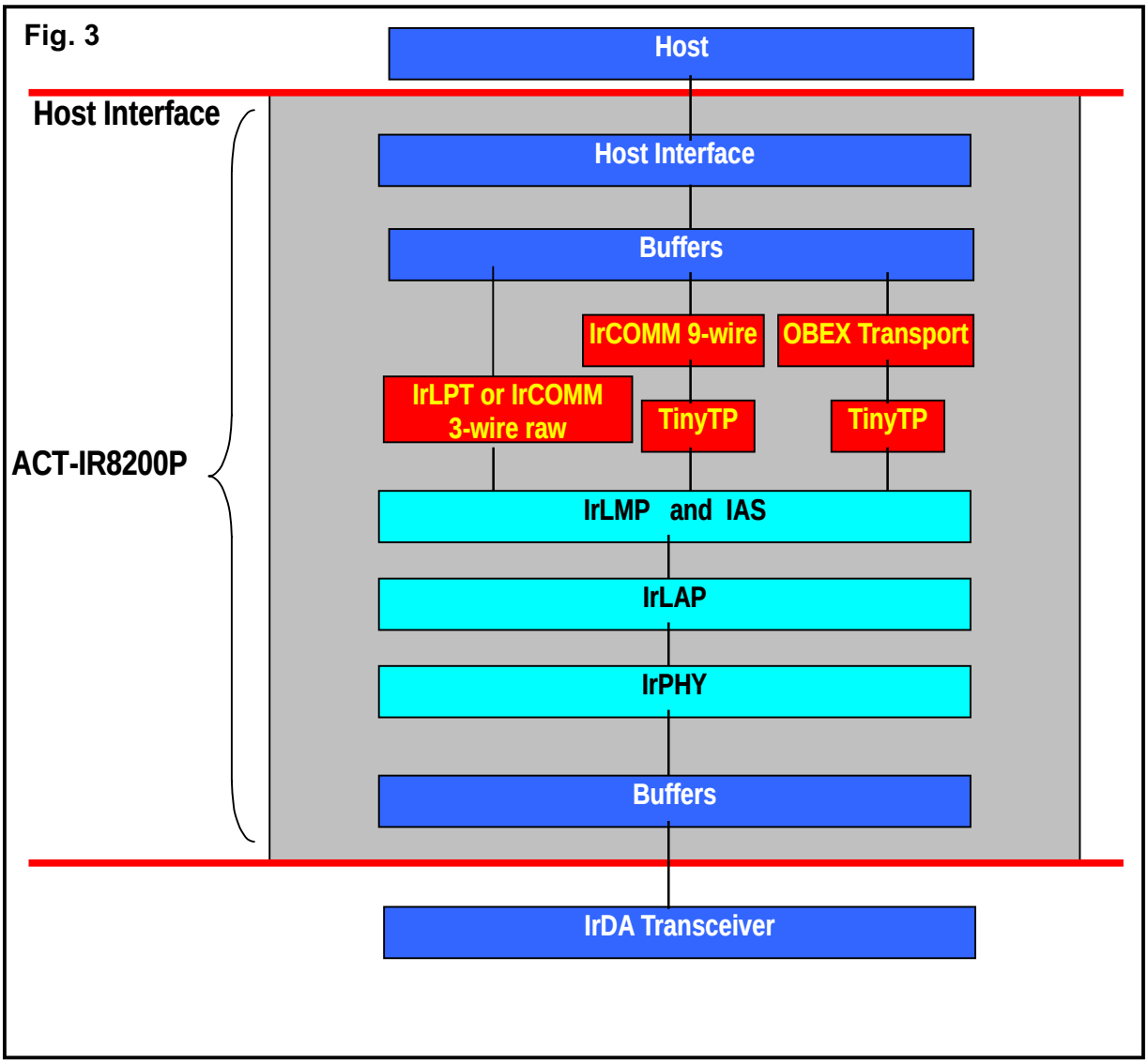
When ACT-IR8200P is used as the only processor in a small-embedded system. There is no host interface and all the uncommitted on-chip resources can be utilized by additional firmware. Actisys offers service of firmware development. This is shown in Fig. 2.

Fig.2 Single processor embedded system



4. Embedded Firmware

Fig. 3 is the block diagram of ACT-IR8200P firmware. The mandatory IrDA protocol layers, IrPHY, IrLAP (comply with TEST frame capability requirement) and IrLMP (including IAS) are handled by ACT-IR8200P. In addition, TinyTP, IrCOMM, IrLPT and IrOBEX transport are all optional for customer choosing, it depends on what customer needs. It can be only IrLPT protocol, TinyTP with IrCOMM 9-wire protocol or all of them.



Because there are several optional IrDA protocols can be implemented into ACT-IR8200P chip, the following are the variation that firmware could be. When you order the chip or evaluation board, IR100SP, you should specify which specific IrDA protocol layer you need. The appropriate ACT-IR8200P with your designated protocol layer will be delivered.

4.1 ACT-IR8200P-P (IrLPT only)

This firmware is using to connect ACT-IR8200P chip to a serial printer without IrDA protocols**,** let the serial printer comes with IrDA IrLPT capability. Following are its features,

- Host data baud rate is 9.6kbit/s,8 data bits,no parity,1 stop bit are used.
- IrPHY interfaces directly to Infrared transceivers for data rate up to 115.2 kbit/s (9.6kbit/s, 19.2kbit/s, 38.4kbit/s, 57.6kbit/s, 115.2kbit/s)
- Two kinds of flow-control are using, When the host is busy and cannot accept more data from TX, there are two ways to suspend ACT-IR8200P from sending more TX,

  Hardware: Drive STOP_TX high. If this is not used, STOP_TX must be strapped low.
  Software: Send a Ctrl-S (X-off, 0x13) byte to RX for suspend, and any other byte to resume. If this method is not used, Rx should be strapped to high (idle).

4.2 ACT-IR8200P-C (TinyTP + IrCOMM)

This firmware is using to connect ACT-IR8200P chip to a serial device with UART interface**,** let the serial device comes with IrCOMM 9-wire cooked and IrCOMM 3-wire cooked. Following are its features,

- Host data baud rate is 9.6kbit/s, 8 data bits, no parity and 1 stop bit are used.
- IrPHY interfaces directly to Infrared transceivers for data rate up to 57.6 kbit/s (9.6kbit/s, 19.2kbit/s, 38.4kbit/s, 57.6kbit/s).
- Hardware flow-control are using, When the host is busy and cannot accept more data from TX, drive STOP_TX high to suspend ACT-IR8200P from sending more TX. If this is not used, STOP_TX must be strapped low.

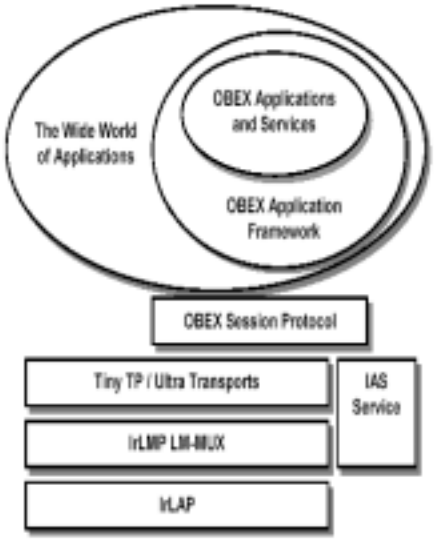
4.3 ACT-IR8200P-B (TinyTP + IrOBEX Transport)

This firmware is using to connect ACT-IR8200P chip to a serial device with UART interface**,** let the serial device comes with IrOBEX transport capability. Following are its features,

- Host data baud rate is 9.6kbit/s, 8 data bits, no parity and 1 stop bit are used.
- IrPHY interfaces directly to Infrared transceivers for data rate up to 57.6 kbit/s (9.6kbit/s, 19.2kbit/s, 38.4kbit/s, 57.6 kbit/s)

- IrOBEX transport is not IrOBEX. The difference between "IrOBEX transport" and "IrOBEX" is that they work on different layer. According to IrOBEX specification from IrDA website, section 1.2 on page 10 says: "The IrOBEX specification consists of two major parts: a protocol and an application framework." This is also illustrated graphically on below. The "protocol" part is presented in five rectangles at the lower half of this figure, these five rectangles are necessary for IrDA communication. The "application framework" is resented in ellipses inside the "wide word of applications" at the upper half of this figure, these parts are the exact place that handles the IrOBEX transaction.

  IrOBEX transport means that ACT-IR8200P-B supports protocol part of IrOBEX only, and it



doesn't and can't provide the "application

framework" part of IrOBEX in the "wide world of applications" (the ellipses in Figure). ACT-IR8200P-B will passes all the payloads of IrOBEX to the host system, the host system using our dongle or chip must do that part themself. ACTiSYS currently does not do any application software, and cannot provide examples of IrOBEX applications.

- Hardware flow-control are using, when the host is busy and cannot accept more data from TX, drive STOP_TX high to suspend ACT-IR8200P from sending more TX. If this is not used, STOP_TX must be strapped low.

5. Implementation information

Following signal lists descript the implementation notes when designed into board.

(1) Power supply

Pin	Name	Comments
1	DVcc	Digital power. Connect a 0.1uF bypass capacitor at this pin.
64	AVcc	Analog power. Connect a 0.1uF bypass capacitor at this pin.
62	AVss	Analog ground
63	DVss	Digital ground

(2) Crystal Oscillator

Pin	Name	Comments
53	XTIN	Input port for crystal oscillator. Only standard crystals can be connected.
52	XTOUT	Output terminal of crystal oscillator

Both of these two pins connect a 20pF capacitor.

(3) Reset

Pin	I/O type	Name	Comments
58	I	/RST	Active low reset. This signal can be generated by the host, a RC circuit or a RESET chip. It supports Brown-out feature.

(4) IrDA Transceiver

Pin	I/O type	Name	Comments
19	O	Ir_TX	IrDA Transmitter, high active. Connect to TXD pin of IrDA transceiver.
15	I	/Ir_RX	IrDA Receiver, active low. Connect to RXD pin of IrDA transceiver.

Please see the transceiver's specification to get more detail information about transceiver.
Place IR8200P chip next to transceiver module as close as possible. And keep chip away from high power consumption components.

(5) Visual LED Drive

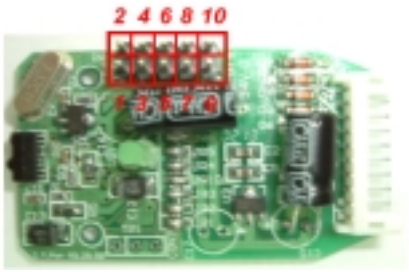
Pin	I/O type	Name	Comments
35	O	/LED	Optional LED. Active low. This is optional and application dependent. Open it if not used.

(6) Host Interface

Pin	I/O type	Name	Comments
32	O	TX	Serial output to Host. Active low.
30	I	STOP_TX	Flow control input from Host. Pull high to stop IR8200P chip sending data to host. Pull it low if not used.
33	I	RX	Serial input from Host. Pull high if not used.
31	O	STOP_RX	Flow control output to Host. Pull high to stop host device sending data to IR8200P chip. Open it if not used.
34	I	Reserve	Pull high or low if not used.
29	O	Reserve	Open if not used.
28	I	Reserve	Pull high or low if not used.
12	I	Reserve	Pull high or low if not used.

(7) Auxiliary Port

Pin No	Name	Pin No	Name
2	57 TCK	**1**	13 Aux_out
4	58 /RST	**3**	22 Aux_in
6	VCC	**5**	GND
8	NC	**7**	NC
10	NC	**9**	NC



This Auxiliary Port is optional but recommended to facilitate in-system firmware update. A 10-pin 2x5 header is recommended:

(8) Other IR8200P pins

Pins 8, 10, 11, and 25 should be grounded. All other unused pins may be open.

6. PIN Description

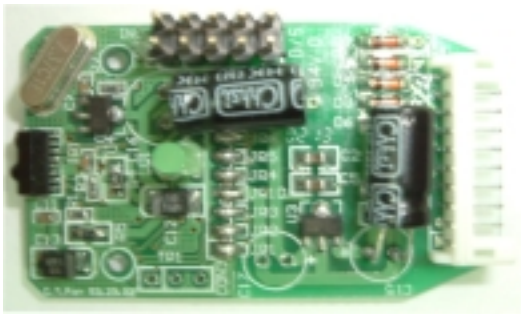
Symbol	Pin No.	I/O Type	Descriptions
AVcc	64		Analog supply voltage, positive terminal.
Avss	62		Analog supply voltage, negative terminal.
DVcc	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DVss	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0	12	I/O	General digital I/O pin.
P1.1	13	I/O	General digital I/O pin. Aux_out for in-system firmware update
P1.2	14	I/O	General digital I/O pin.
P1.3	15	I	Ir_RX. IR signal input from IrDA transceiver.
P1.4	16	I/O	General digital I/O pin.
P1.5	17	I/O	General digital I/O pin.
P1.6	18	I/O	General digital I/O pin.
P1.7	19	O	Ir_TX. IR signal output to IrDA transceiver.
P2.0	20	I/O	General digital I/O pin.
P2.1	21	I/O	General digital I/O pin.
P2.2	22	I/O	General digital I/O pin. Aux_in for in-system firmware update
P2.3	23	I/O	General digital I/O pin.
P2.4	24	I/O	General digital I/O pin.
P2.5	25	I/O	General digital I/O pin.
P2.6	26	I/O	General digital I/O pin.
P2.7	27	I/O	General digital I/O pin.
P3.0	28	I/O	General digital I/O pin.
P3.1	29	I/O	General digital I/O pin.
P3.2	30	I	STOP_TX. Flow control input from Host.
P3.3	31	O	STOP_RX. Flow control output to Host.
P3.4	32	O	SOUT. Send data to host
P3.5	33	I	SIN. Receive data from host
P3.6	34	I/O	General digital I/O pin.
P3.7	35	I/O	General digital I/O pin.
P4.0	36	I/O	General digital I/O pin.
P4.1	37	I/O	General digital I/O pin.
P4.2	38	I/O	General digital I/O pin.
P4.3	39	I/O	General digital I/O pin.
P4.4	40	I/O	General digital I/O pin.
P4.5	41	I/O	General digital I/O pin.
P4.6	42	I/O	General digital I/O pin.
P4.7	43	I/O	General digital I/O pin.

Symbol	Pin No.	I/O Type	Descriptions
P5.0	44	I/O	General digital I/O pin.
P5.1	45	I/O	General digital I/O pin.
P5.2	46	I/O	General digital I/O pin.
P5.3	47	I/O	General digital I/O pin.
P5.4	48	I/O	General digital I/O pin.
P5.5	49	I/O	General digital I/O pin.
P5.6	50	I/O	General digital I/O pin.
P5.7	51	I/O	General digital I/O pin.
P6.0	59	I/O	General digital I/O pin.
P6.1	60	I/O	General digital I/O pin.
P6.2	61	I/O	General digital I/O pin.
P6.3	2	I/O	General digital I/O pin.
P6.4	3	I/O	General digital I/O pin.
P6.5	4	I/O	General digital I/O pin.
P6.6	5	I/O	General digital I/O pin.
P6.7	6	I/O	General digital I/O pin.
/RST	58	I	Reset input, nonmaskable interrupt input port, or bootstrap loader start (in Flash devices).
TCK	57	I	Test clock. TCK is the clock input port for device programming test and bootstrap loader start (in Flash devices).
TDI	55	I	Test data input. TDI is used as a data input port. The device protection fuse is connected to TDI.
TDO	54	I/O	Test data output port. TDO/TDI data output or programming data input terminal
TMS	56	I	Test mode select. TMS is used as an input port for device programming and test.
VeREF+	10	I	Input for an external reference voltage to the ADC
VREF+	7	O	Output of positive terminal of the reference voltage in the ADC
VREF-	11	O	Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
XTIN	53	I	Input port for crystal oscillator XT. Only standard crystals can be connected.
XTOUT	52	O	Output terminal of crystal oscillator XT

7. Evaluation Board or Ready IrDA-Compliant Internal PCB:

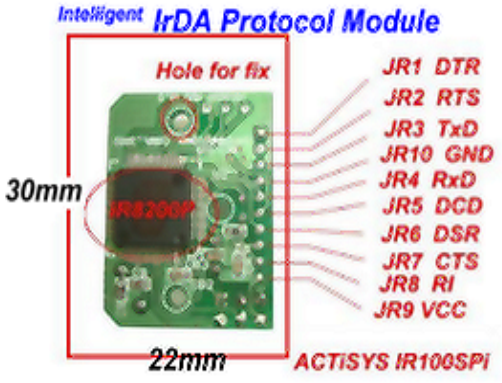
It is recommended that you verify the compatibility with your host system by using our IrDA Protocol to RS232 Adapter, ACT-IR100SP. This is a self-content unit, with ACT-IR8200P, IrPHY components, RS232-level converters and external AC power source, all built into a compact package. Also available for quick IrDA implementation is the internal PCB version. ACT-IR100SPi dongle which enables your host system to be IrDA (IrReady) certifiable, immediately. Moreover, this internal PCB can be full PCB with RS232 interface circuitry, or as half-PCB with TTL-level SCI interface, without the burden of RS232 interface circuitry.

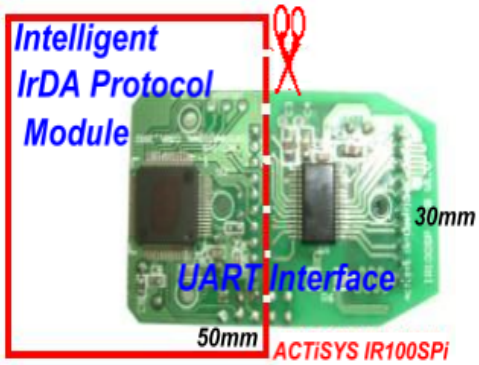
ACT-IR100SP is designed to enable instant IrDA capability of your host via RS232 serial port; e.g. modem, serial printer, instrumentation, meter, data terminal and medical device. Once ACT-IR100SP is proven to work well with your host system, and upon execution of mutual NDA and purchasing terms, we'll provide circuit diagrams to help speed up your implementation.



IR8200P PCB - Top Side

IR8200P PCB - Reverse Side





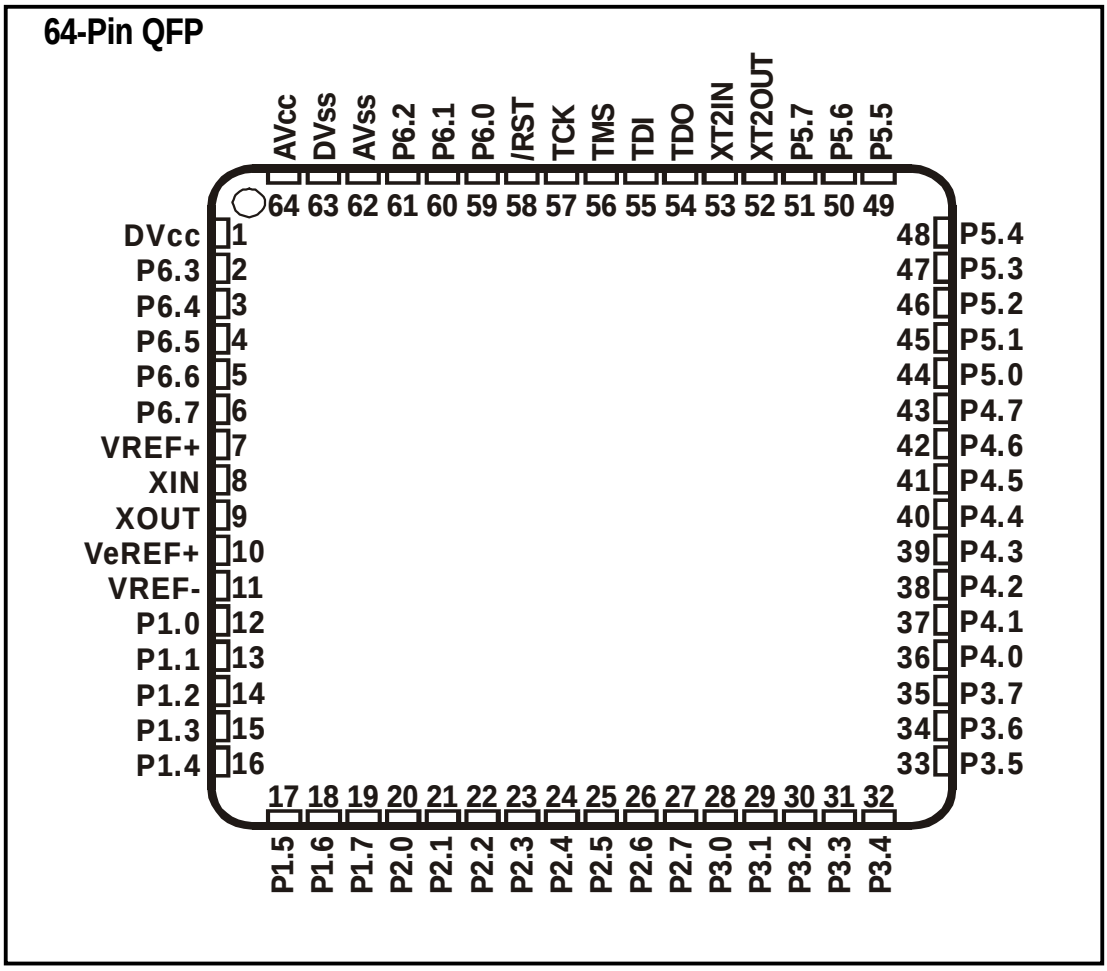
8. Packages:

- QFP 64

DC electrical characteristics:
- Operating voltage: 2.7 ~ 3.6 VDC
- Operating current: 2uA (Standby Mode)

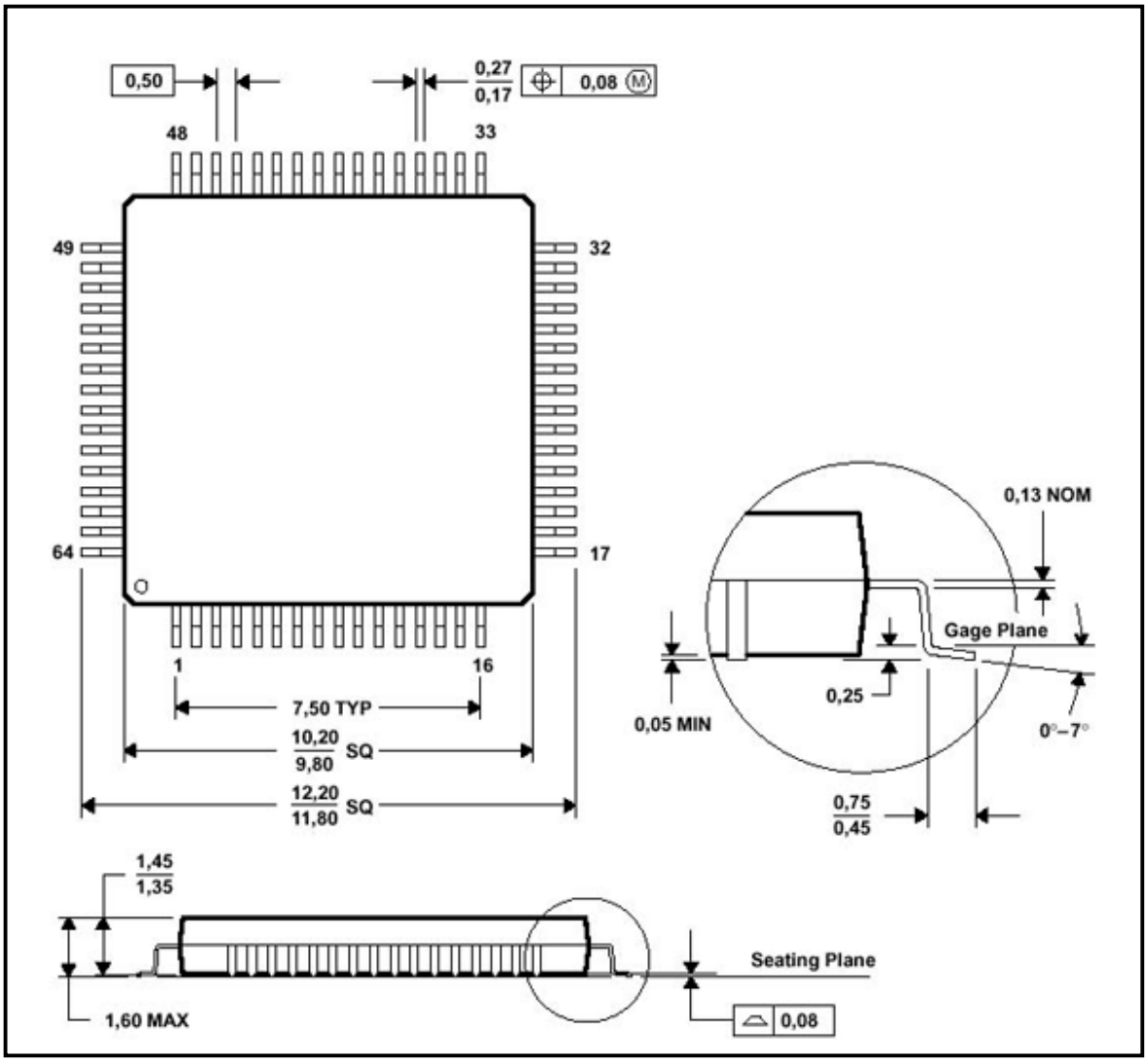
Operating temperature:
- -40℃ ~ +85℃.

Storage temperature:
- -55℃ ~ +150℃



9. Package Dimensions

64-PIN QFP



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.