48511 Warm Springs Blvd., Suite 206, Fremont, CA 94539
Tel: (510) 490-8024 Fax: (510) 623-7268
Website: http://www.actisys.com E-mail: irda-info@actisys.com

ACT-IR8200P/M

IrDA Compliant Protocol Processor

Preliminary Specification

Apr. 25, 2003 Rev.0.4

ACTiSYS reserves the right to make changes without further notice to any products herein to improve reliability, function or design. ACTiSYS does not assume any liability arising out of the application or use of any product or circuit described herein.

Revision History		
Revision	**Date**	**Comment**
Rev. 0.0	02/28/2002	Draft Preliminary Design Specification for internal review.
Rev. 0.0a	06/10/2002	Draft Preliminary Design Specification for internal review.
Rev. 0.1	06/24/2002	Reviewed by Lichen Wang
Rev. 0.1a	11/29/2002	Reviewed by Lichen Wang
Rev. 0.2	12/20/2002	Add implementation information.
Rev. 0.2a	12/31/2002	Modify IrDA port baud rate and flow control for each firmware
Rev. 0.2b	01/13/2003	Modify host baud rate for each firmware.
Rev. 0.3	04/16/2003	Add definition for new firmware combination.
Rev. 0.4	04/25/2003	Reviewed by Dr. Wang

Table of Contents

1. Introduction

ACT-IR8200P/M is a low cost, high-integration and field programmable microprocessor with on-chip IrDA primary and secondary protocol stack and on-chip Infrared physical encoder/ decoder. It offers Infrared communication capability to embedded devices, making these devices immediately IrDA capable, without having to port IrDA protocol to the host devices.

2. Features

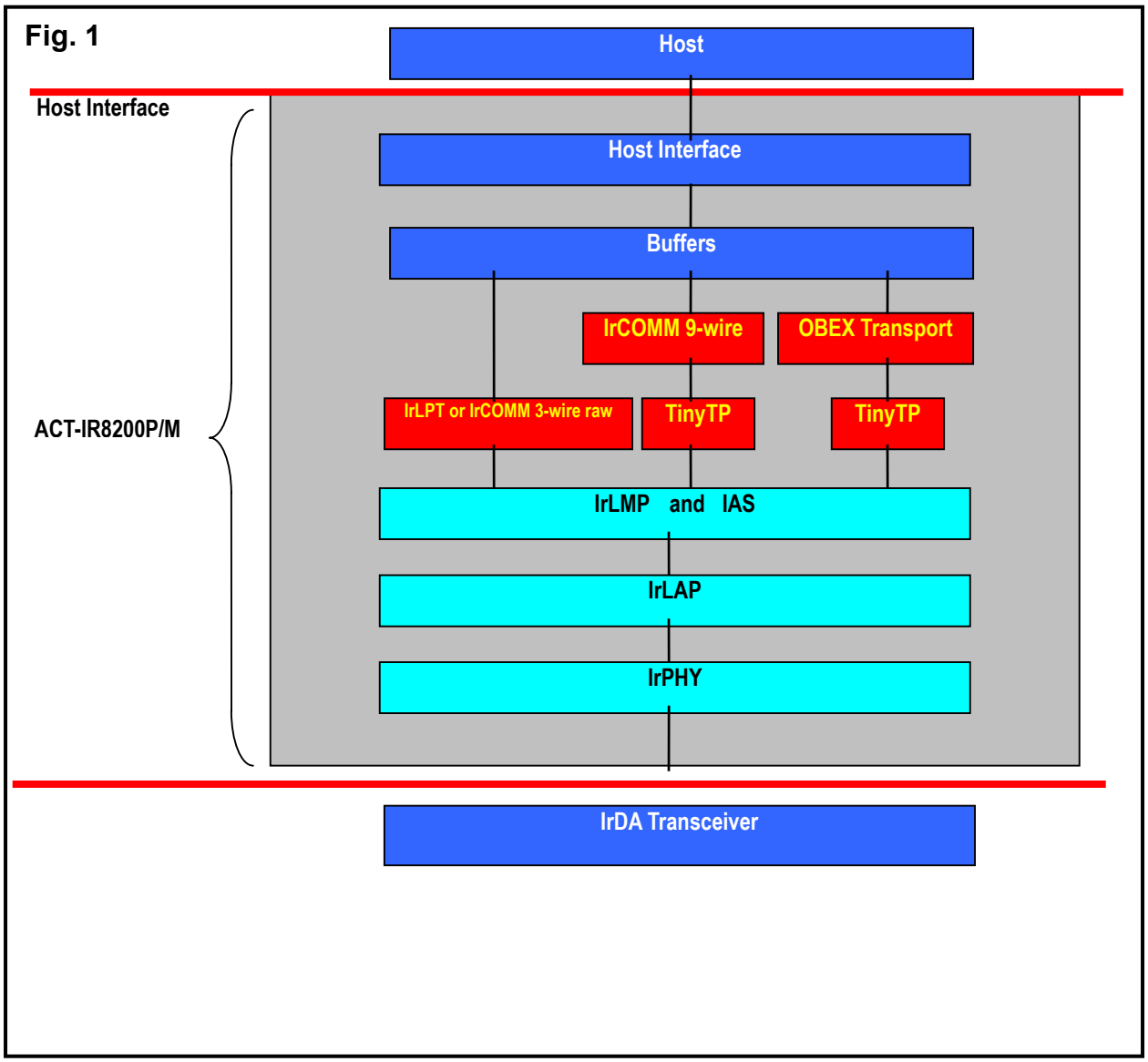
- A complete IrDA Protocol stack in a single chip.
- Includes IrPHY encoding/decoding and interfaces directly to Infrared transceivers for data rate up to 115.2kbit/s. Only an external Infrared transceiver is needed to complete an IrDA compliant infrared communication subsystem.
- Off-the-shelf, semi-custom, or full-custom firmware in on-chip Flash EPROM.
- Supports both IrDA Primary and Secondary mode.
- Supports host baud rate from 9.6kbit/s to 115.2kbit/s.
- Low supply voltage, 3.0 V to 3.6 V.
- Low current consumption, 2uA standby, 3mA active.
- Small low profile plastic 64-pin QFP package.
- Choice of different amount of on-chip RAM and Flash EPROM to optimize cost and performance.
- Available in programmed and tested chips, assembled & tested boards, or fully packaged devices.
- Abundant uncommitted on-chip resources can be utilized to implement a small complete embedded system by itself without a host CPU.
  - 46 uncommitted digital I/O pins
  - 8 of the uncommitted I/O pins can also be used by on-chip 12-bit ADC for embedded functions.
  - Uncommitted on-chip USART supports full duplex asynchronous serial communication. It also supports 3-wire or 4-wire synchronous peripheral interface (SPI).
  - Uncommitted on-chip 16-bit timer with 3 channels of versatile compare/capture blocks.
  - Uncommitted 32.768 kHz low power oscillator.
  - Low power standby with wake-up from IR, low power oscillator, and
  - Other sources.

- A ready IrDA-compatible CMOS board and RS232 dongle for SCI interface are available:
  CMOS board: ACT-IR100SP/Mi
  RS232 dongle: ACT-IR100SP/M

3. Firmware architecture

Fig. 1 is the block diagram of ACT-IR8200P/M firmware architecture. The mandatory IrDA protocol layers, IrPHY, IrLAP (comply with TEST frame capability requirement) and IrLMP (including IAS) are handled by ACT-IR8200P/M. In addition, TinyTP, IrCOMM 9-wire, IrLPT(3 wire raw) and OBEX transport are all optional for customer choosing, it depends on what customer needs. It can be only IrLPT protocol, TinyTP with IrCOMM 9-wire protocol or all of them.

Fig. 1



4. Off-the-shelf firmware

There are various Off-the-shelf firmware are available and shown in following table for customer biggest flexibility:

Part No. ACT-IR8200P/ M-###	Protocol in Primary	Protocol in Secondary	Host baud rate	Data format	Max. IrDA baud rate	Chip capability
101		IrLPT	9.6kbit/s—115.2kbit/s	7/8,N/E/O,1/2	115.2kbit/s	133
201		IrCOMM	9.6kbit/s—115.2kbit/s	7/8,N/E/O,1/2	115.2kbit/s	133
301		OBEX transport	9.6kbit/s—115.2kbit/s	8,N/E/O,1/2	115.2kbit/s	133
401	IrLPT	optional	9.6kbit/s—115.2kbit/s	7/8,N/E/O,1/2	115.2kbit/s	147
501	IrCOMM	optional	9.6kbit/s—115.2kbit/s	7/8,N/E/O,1/2	115.2kbit/s	147
601	OBEX transport	optional	9.6kbit/s—115.2kbit/s	8,N/E/O,1/2	115.2kbit/s	147

All the combination can be chose from table above, the following are detailed description:

a. Protocol in Primary: It will initial the communication with a Secondary device and ask for this kind of specified protocol service.
b. Protocol in Secondary: It supports this specified protocol for Primary device to ask for and to communicate with.
c. Host baud rate: UART baud rate. Specify this connect to host. It is fixed, means it can be changed by user but by ACTiSYS. See chapter “Host Interface” below to get more detailed.
d. Data format: Data bits can be 7 or 8, parity bit can be None/Even/Odd, stop-bit can be 1 or 2.
e. Max IR baud rate: IR8200P/M supports SIR baud rate up to 115.2kbit/s.
f. Chip capability: This is a comment for different on-chip RAM. For ACTiSYS use only.

Any unlisted but needed protocol can be supported by ACTiSYS, please contact ACTiSYS to get more information.

5. Host Interface

Asynchronous serial interface is used to interface with the Host, the following lists the default setting:

- Data rate: 115.2 kbit/s
- Data bits: 8-bit
- Parity: None
- Stop bits: 1-bit
- Signal level: 3.3V CMOS for Chips and CMOS boards, RS232 for RS232 dongles and devices
- Flow-control: Hardware flow control unless specifically stated otherwise

Asynchronous serial interfaces with settings other than listed above, as well as other kinds of host interfaces are also possible.

There are a total of 10 signals between the host and the chip/board/device, (Where chip/board/device mean ACT-IR8200P/M/ACT-IR100SP/Mi/ACT-IR100SP/M). The pin assignment and name of each signal at the chip/board/device levels are summarized in Table 1 below. Please note that DTE nomenclature is used to name these signals on the RS232 board or device. In order to connect them to another DTE, a Null-Modem must be used in-between. The pin assignment and name after the Null-Modem are also listed in this table.

Table 1: Host interface signals

I/O type	ACT-IR8200P/M chip		ACT-IR100SP/ Mi board		ACT-IR100SP/M board		RS232 dongle		Null-Modem	
	Pin[1]	Name	Pin[2]	Name	Pin[3]	Name	Pin[4]	Name	Pin[5]	Name
O	29	Status	1	Status	1	DTR	4	DTR	6	DSR
O	31	Stop-Rx	2	Stop-Rx	2	RTS	7	RTS	8	CTS
O	32	Tx	3	Tx	3	TxD	3	TX	2	RxD
Gnd	62+63	Ground	4	Ground	4	Gnd	5	Gnd	5	Gnd
I	33	Rx	5	Rx	5	RxD	2	RxD	3	TxD
I	28	Control-2	6	Control-2	6	DCD	1	DCD	---	---
I	34	Control-1	7	Control-1	7	DSR	6	DSR	4	DTR
I	30	Stop-Tx	8	Stop-Tx	8	CTS	8	CTS	7	RTS
I	12	Control-3	9	Control-3	9	RI	9	RI	---	---
Pwr	1+64	Power 3V	10	Power 3V	10	Ext Pwr 5V-12V	Pigtail	Ext Pwr 5V-12V	---	---

1. At chip level, the pin assignment refers to the pin number of the 64-pin QFP package of the chip.
2. At CMOS board level, the pin assignment refers to the pin number of the 10-pin CON3 connector.
3. At RS232 board level, the pin assignment refers to the pin number of the 10-pin CON2 connector.
4. At RS232 device level, the pin assignment refers to the pin number of the DB-9P male connector.
5. The pin assignment under Null-Modem refers to the pin number of the DB-9S female connector.

Normal usage of Host interface signals

(Note that "loop-back" from **DTR** to **DSR** or from **RTS** to **CTS** will not work. See details below.)

Rx/RxD: This input signal is used by the chip/board/device to receive serial data from the host. For IrLPT Secondary only, it is used to receive X-on or X-off from the host (usually a printer) to start/stop **Tx/TxD** output (software flow-control). If not used, the CMOS **Rx** input should be driven high, the RS232 **RxD** input should be driven low. If a Null-Modem is used, the signal from the host is called **TxD**.

Stop-Rx/RTS: This output signal is used by the chip/board/device to notify the host not to send more **Rx/RxD** (hardware flow-control). If the host ignores this, input data **Rx/RxD** may be lost due to buffer overflow. If a Null-Modem is used, the signal to the host is called **CTS**.

Tx/TxD: This output signal is used by the chip/board/device to send serial data to the host. For IrLPT Primary only, it is used to send X-on or X-off to the host to start/stop **Rx/RxD** input (software flow-control). If a Null-Modem is used, the signal to the host is called **RxD**.

Stop-Tx/CTS: This input signal is sensed by the chip/board/device to stop sending **Tx/TxD** to avoid host buffer overflow. If the host does not need this, the CMOS **Stop-Tx** input should be driven low, the RS232 input **CTS** should be driven high. If a Null-Modem is used, the signal from the host is called **RTS**.

Status/DTR: This output signal is used by the chip/board/device to notify the host that an IrDA connection is active. If a Null-Modem is used, the signal to the host is called **DSR**.

Control-1/DSR: This input signal is sensed by the chip/board/device to enable or disable IrDA connection. If the host does not need this, the CMOS **Control-1** input should be driven low, the RS232 input **DSR** should be driven high. If a Null-Modem is used, the signal from the host is called **DTR**.

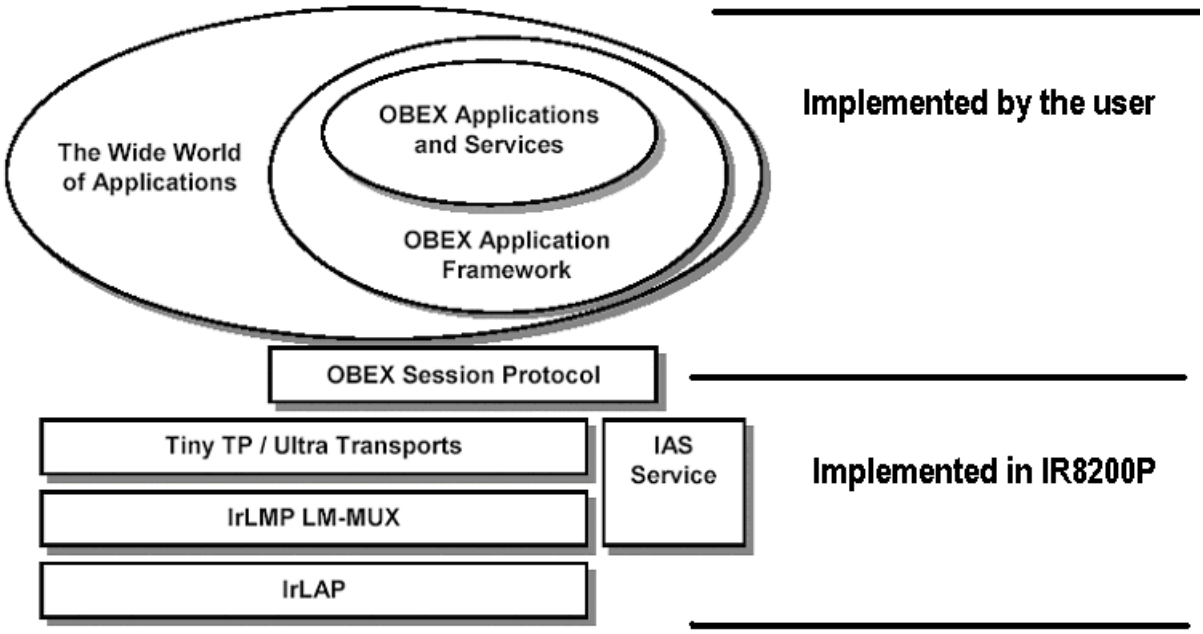
Control-2/DCD: This input signal is normally not used. The CMOS **Control-2** input should be driven high. The RS232 **DCD** input need not be connected.

Control-3/RI: This input signal is normally not used. The CMOS **Control-3** input should be driven high. The RS232 **RI** input need not be connected.

6. OBEX transport Description

The OBEX specification consists of two major parts: a protocol and an application framework. This is also illustrated graphically below. The "application framework" is represented in ellipses inside the "wide word of applications" at the upper half of this figure. The "protocol" part is presented in five rectangles at the lower half of this figure.

ACT-IR8200P/M doesn't and can't provide the "application framework" part of OBEX in the "wide world of applications" (the ellipses in Figure). The host system using IR8200P/M must implement that part itself.



7. Implementation notice

Following signal lists the description of implementation notes when designed into board.

(1) Power supply

Pin	Name	Comments
1	DVcc	Digital power. Connect a 0.1uF bypass capacitor at this pin.
64	AVcc	Analog power. Connect a 0.1uF bypass capacitor at this pin.
62	AVss	Analog ground
63	DVss	Digital ground

(2) Crystal Oscillator

Pin	Name	Comments
53	XTIN	Input port for crystal oscillator. Only standard crystals can be connected.
52	XTOUT	Output terminal of crystal oscillator
25	P2.5	Internal clock input. Connect 100K ohm resistor to VCC.

Both of these two pins connect a 20pF capacitor.

(3) Reset

Pin	I/O type	Name	Comments
58	I	/RST	Active low reset. This signal can be generated by the host, a RC circuit or a RESET chip. It supports Brownout feature.

(4) IrDA Transceiver

Pin	I/O type	Name	Comments
19	O	Ir_TX	IrDA Transmitter, high active. Connect to TXD pin of IrDA transceiver.
15,36	I	/Ir_RX	IrDA Receiver, active low. Connect to RXD pin of IrDA transceiver.
27	O	IR_VCC	Transceiver power supports.

Please see the transceiver's specification to get more detail information about transceiver.
Place IR8200P/M chip next to transceiver module as close as possible. And keep chip away from high power consumption components.

(5) Visual LED Drive

Pin	I/O type	Name	Comments
35	O	/LED	Optional LED. Active low. This is optional and application dependent.

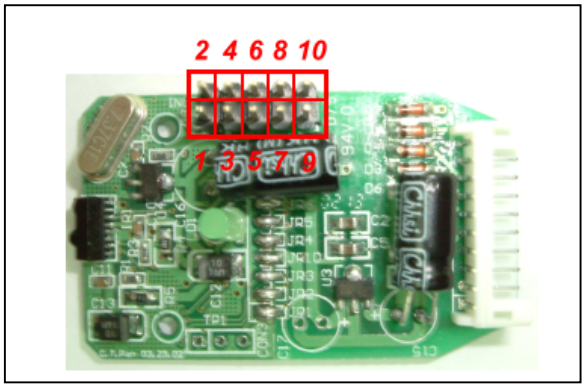
(6) Host Interface

Pin	I/O type	Name	Comments
32	O	TX	Serial output to Host. Active low.
30	I	STOP_TX	Flow control input from Host. Pull high to stop IR8200P/M chip sending data to host. Pull it low if not used.
33	I	RX	Serial input from Host. Pull high if not used.
31	O	STOP_RX	Flow control output to Host. Pull high to stop host device sending data to IR8200P/M chip. Open it if not used.
34	I	Control-1/DSR	Pull low if not used.
29	O	Status/DTR	Open if not used.
28	I	Control-2/DCD	Ground it if not used.
12	I	Control-3/RI	Ground it if not used.

(7) Auxiliary Port

The following table is the pin assignment of auxiliary port, which offers the capability of firmware update. It is not necessary to care about this part when implement.

Socket Pin No	Chip pin no	Name	Socket Pin No	Chip pin no.	Name
2	57	TCK	**1**	13	Aux_out
4	58	/RST	**3**	22	Aux_in
6		VCC	**5**		GND
8		NC	**7**		NC
10		NC	**9**		NC



(8) Other IR8200P/M pins

Pins 8,10 and 11 should be grounded. All other unused pins may be open.

8. PIN Description

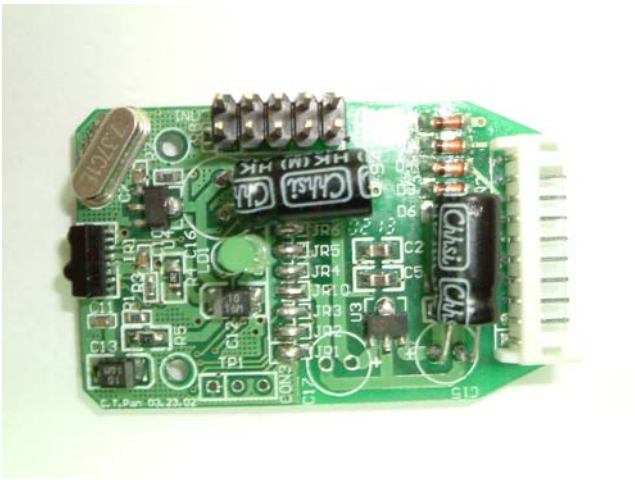
Symbol	Pin No.	I/O Type	Descriptions
AVcc	64		Analog supply voltage, positive terminal.
Avss	62		Analog supply voltage, negative terminal.
DVcc	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DVss	63		Digital supply voltage, negative terminal. Supplies all digital
P1.0	12	I	Control-3/RI.
P1.1	13	I/O	General digital I/O pin. Aux_out for in-system firmware update
P1.2	14	I/O	General digital I/O pin.
P1.3	15	I	Ir_RX. IR signal input from IrDA transceiver.
P1.4	16	I/O	General digital I/O pin.
P1.5	17	I/O	General digital I/O pin.
P1.6	18	I/O	General digital I/O pin.
P1.7	19	O	Ir_TX. IR signal output to IrDA transceiver.
P2.0	20	I/O	General digital I/O pin.
P2.1	21	I/O	General digital I/O pin.
P2.2	22	I/O	General digital I/O pin. Aux_in for in-system firmware update
P2.3	23	I/O	General digital I/O pin.
P2.4	24	I/O	General digital I/O pin.
P2.5	25	I	Internal clock input. Connect 100K ohm resistor to VCC.
P2.6	26	I/O	General digital I/O pin.
P2.7	27	O	IR_VCC. Power for IR transceiver.
P3.0	28	I	Control-2/DCD.
P3.1	29	O	Status/DTR.
P3.2	30	I	STOP_TX. Flow control input from Host.
P3.3	31	O	STOP_RX. Flow control output to Host.
P3.4	32	O	TX. Send data to host
P3.5	33	I	RX. Receive data from host
P3.6	34	I	Control-1/DSR.
P3.7	35	O	/LED.
P4.0	36	I	Ir_RX. IR signal input from IrDA transceiver.
P4.1	37	I/O	General digital I/O pin.
P4.2	38	I/O	General digital I/O pin.
P4.3	39	I/O	General digital I/O pin.
P4.4	40	I/O	General digital I/O pin.
P4.5	41	I/O	General digital I/O pin.
P4.6	42	I/O	General digital I/O pin.
P4.7	43	I/O	General digital I/O pin.

Symbol	Pin No.	I/O Type	Descriptions
P5.0	44	I/O	General digital I/O pin.
P5.1	45	I/O	General digital I/O pin.
P5.2	46	I/O	General digital I/O pin.
P5.3	47	I/O	General digital I/O pin.
P5.4	48	I/O	General digital I/O pin.
P5.5	49	I/O	General digital I/O pin.
P5.6	50	I/O	General digital I/O pin.
P5.7	51	I/O	General digital I/O pin.
P6.0	59	I/O	General digital I/O pin, ADC input.
P6.1	60	I/O	General digital I/O pin, ADC input.
P6.2	61	I/O	General digital I/O pin, ADC input.
P6.3	2	I/O	General digital I/O pin, ADC input.
P6.4	3	I/O	General digital I/O pin, ADC input.
P6.5	4	I/O	General digital I/O pin, ADC input.
P6.6	5	I/O	General digital I/O pin, ADC input.
P6.7	6	I/O	General digital I/O pin, ADC input.
/RST	58	I	Reset input.
TCK	57	I	Reserved.
TDI	55	I	Reserved.
TDO	54	I/O	Reserved.
TMS	56	I	Reserved.
VeREF+	10	I	Input for an external reference voltage to the ADC
VREF+	7	O	Output of positive terminal of the reference voltage in the ADC
VREF-	11	O	Negative terminal for the ADC reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	I/O	Output terminal of crystal oscillator XT1 or test clock input
XTIN	53	I	Input port for crystal oscillator XT. Only standard crystals can be connected.
XTOUT	52	O	Output terminal of crystal oscillator XT

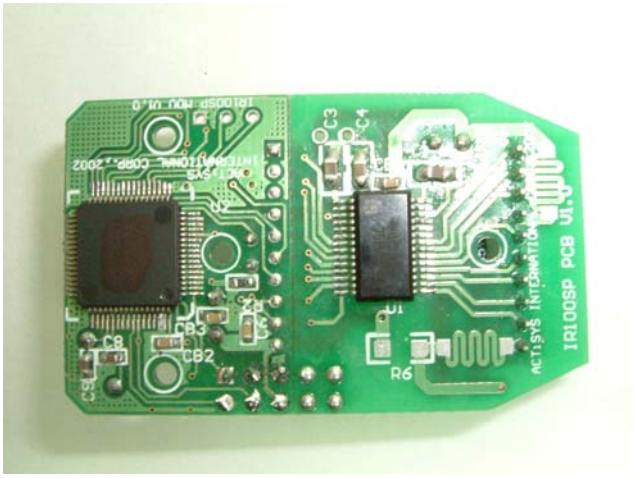
9. Evaluation Board or Ready IrDA-Compliant Internal PCB

It is recommended that you verify the compatibility with your host system by using our IrDA Protocol to RS232 Adapter, ACT-IR100SP/M. This is a self-contained unit, with ACT-IR8200P/M, IrPHY components, RS232-level converters and external AC power source, all built into a compact package. Also available for quick IrDA implementation is the internal PCB version. ACT-IR100SP/Mi dongle which enables your host system to be IrDA (IrReady) certifiable, immediately. Moreover, this internal PCB can be full PCB with RS232 interface circuitry, or as half-PCB with TTL-level SCI interface, without the burden of RS232 interface circuitry.

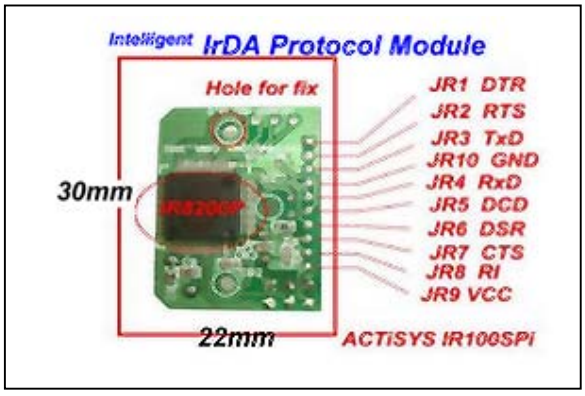
ACT-IR100SP/M is designed to enable instant IrDA capability of your host via RS232 serial port; e.g. modem, serial printer, instrumentation, meter, data terminal and medical device. Once ACT-IR100SP/M is proven to work well with your host system, and upon execution of mutual NDA and purchasing terms, we'll provide circuit diagrams to help speed up your implementation.

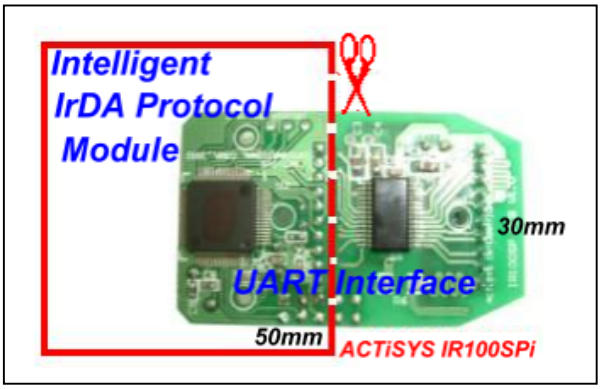


IR100SP/M PCB - Top Side



IR100SP/M PCB - Reverse Side



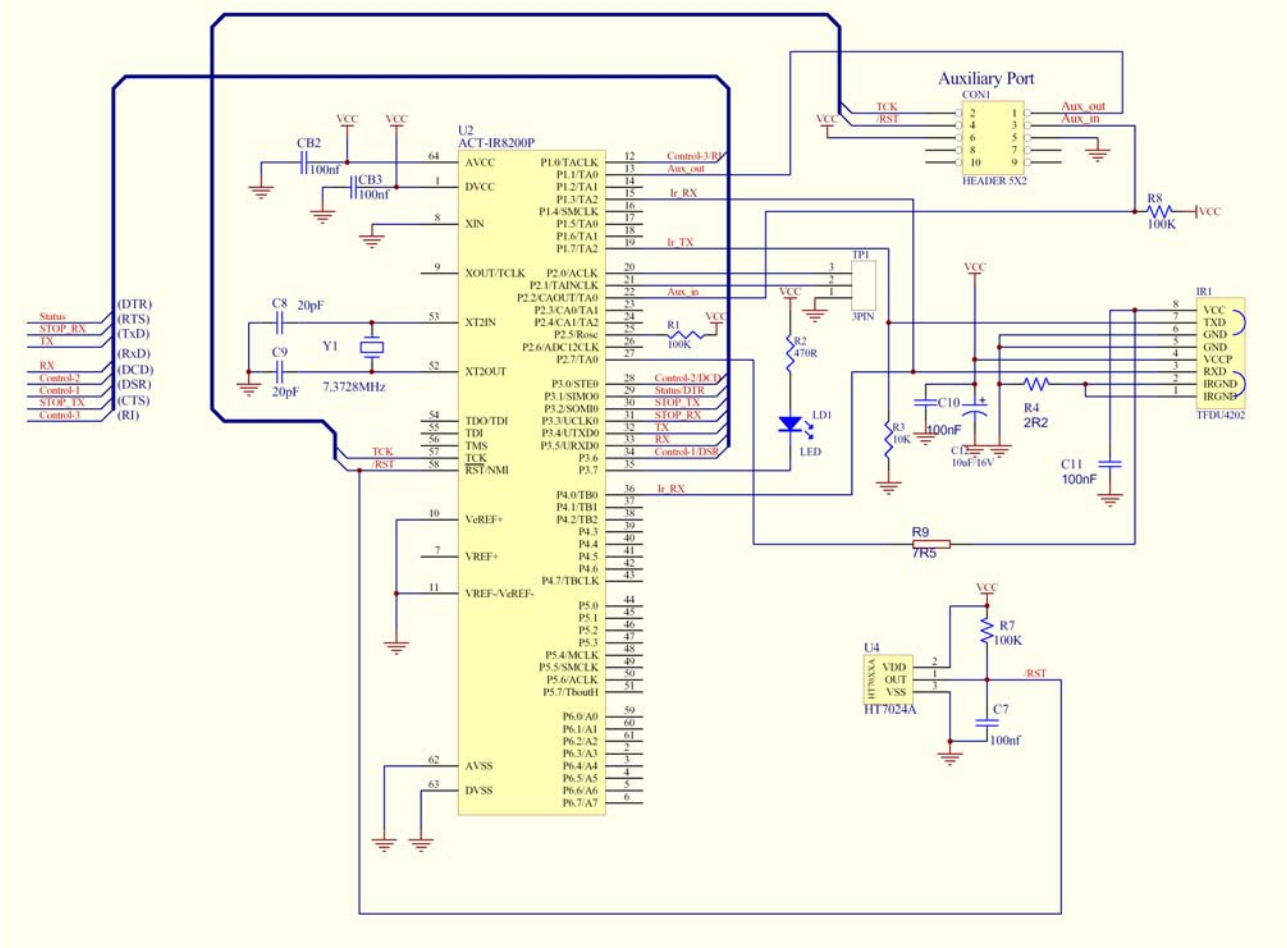


10. Characteristics and Specification

Parameter	MIN.	TYPICAL	MAX.	Units
Supply voltage during program execution, VCC (AVCC = DVCC = VCC)	3.0	3.3	3.6	V
Supply voltage, VSS		0		V
Operating free-air temperature range, TA	-40		85	℃
DC current (Stand-by mode)		2		uA
DC current (Active mode)		3		mA

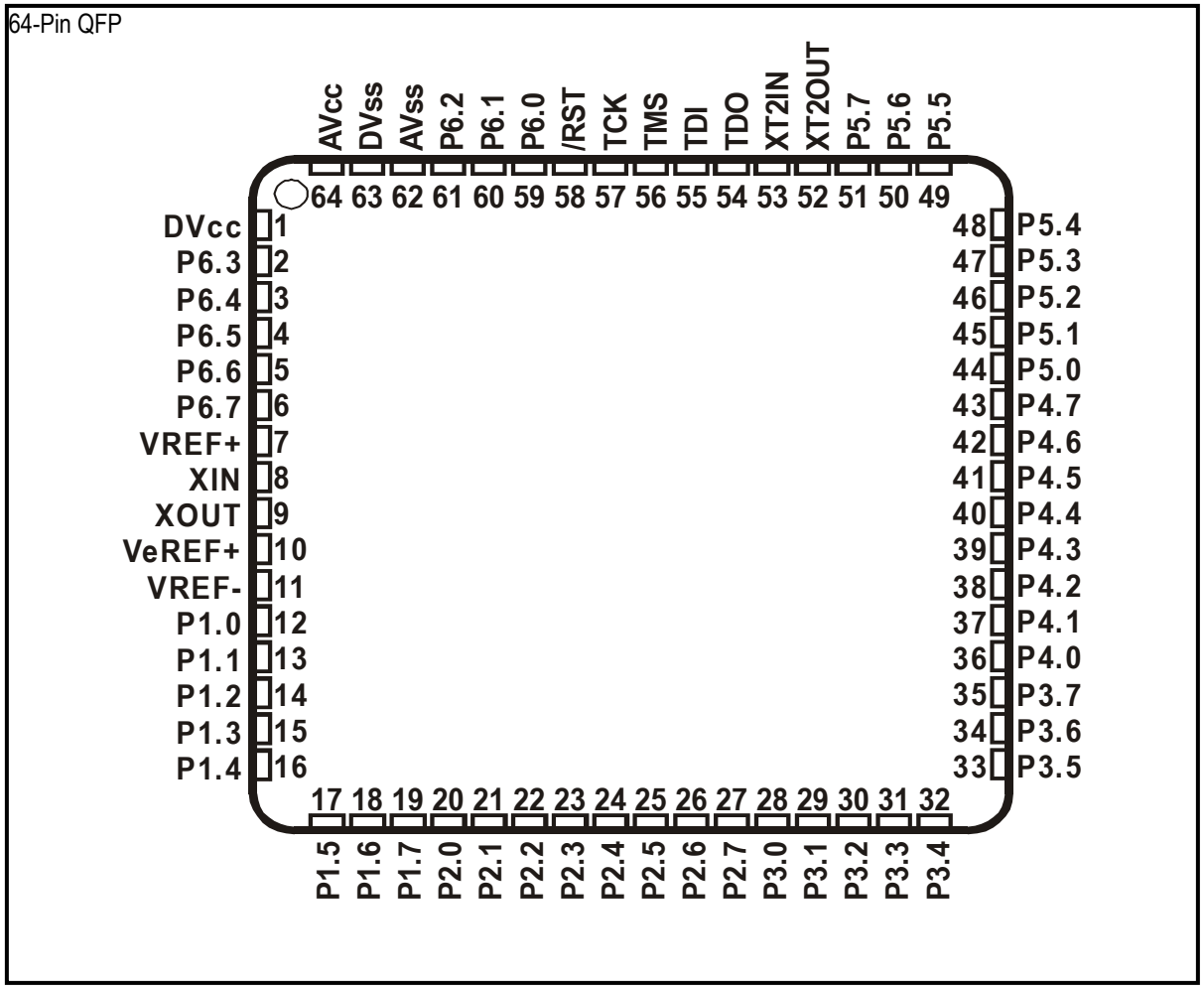
The DC current in active mode is not included transceiver operating current.

11. Application circuit



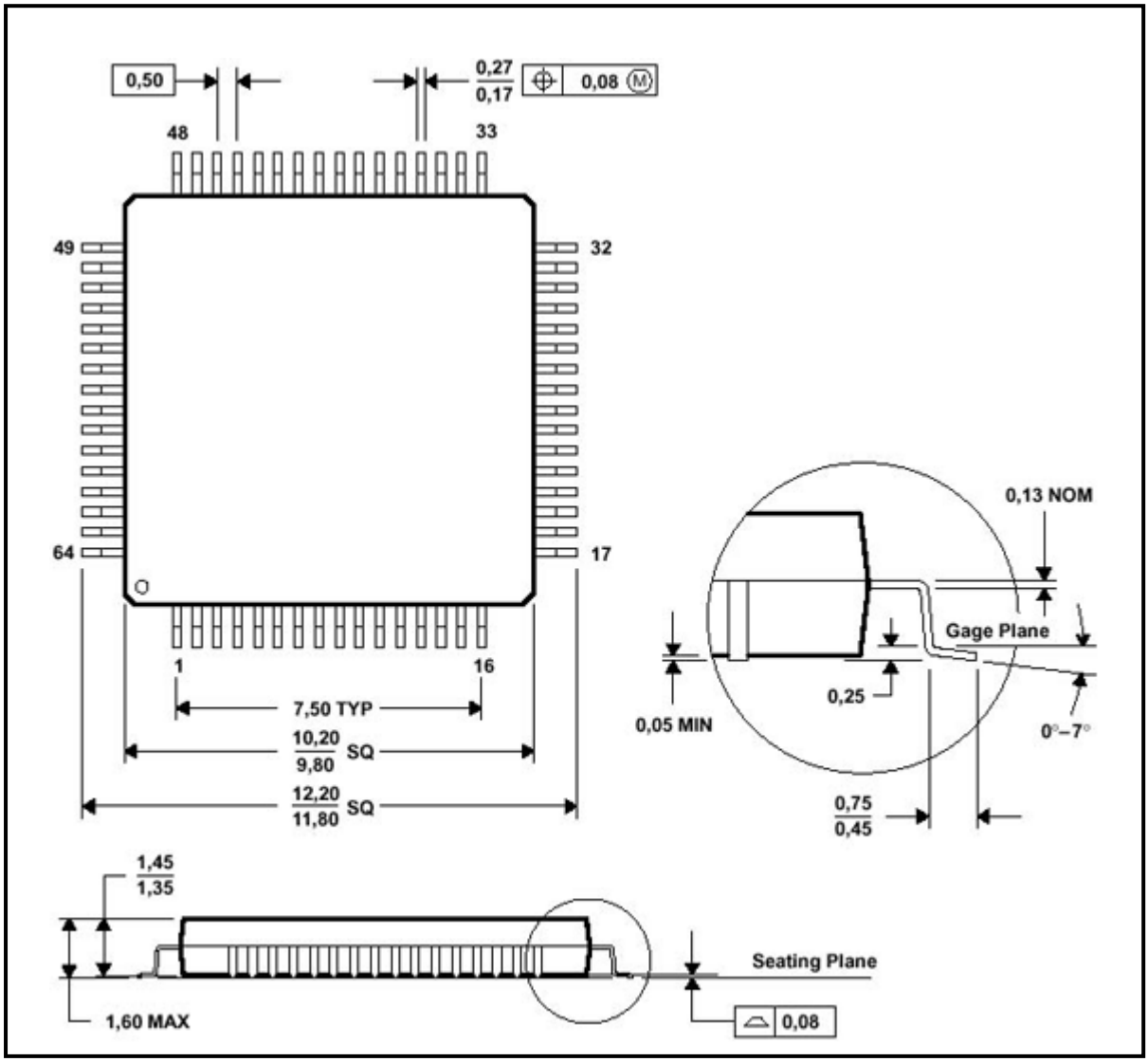
12. Packages

- QFP 64



13. Package Dimensions

64-PIN QFP



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. May also be thermally enhanced plastic with leads connected to the die pads.