ACTiSYS

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ACT-IR8200IC-L

IrDA Compliant Protocol Processor

(IrLAP, IrLMP, TinyTP, etc.)

August 10, 2001 Ver. 0.9g

1. Features

Support IrDA standard including:
- IrLAP
- IrLMP
- TinyTP
- IrCOMM
- IrOBEX transport

Other standards:
- IrLPT

IrDA baud rate supported:
- 9.6kbps
- 19.2kbps
- 38.4kbps
- 57.6kbps
- 115.2kbps

Host Interface:
- Full-duplex asynchronous serial (TxD1, RxD1)
  (Or simplex TxD1 only and software flow control with RxD1.)
- Hardware flow control (RTS1, CTS1)
- Optional line status for link control (DTR1, DSR1)
- Other optional inputs (RI1, CD1)

Host interface baud rate supported:
- 1.2kbps
- 2.4kbps
- 4.8kbps
- 9.6kbps
- 19.2kbps
- 38.4kbps
- 57.6kbps
- 115.2kbps

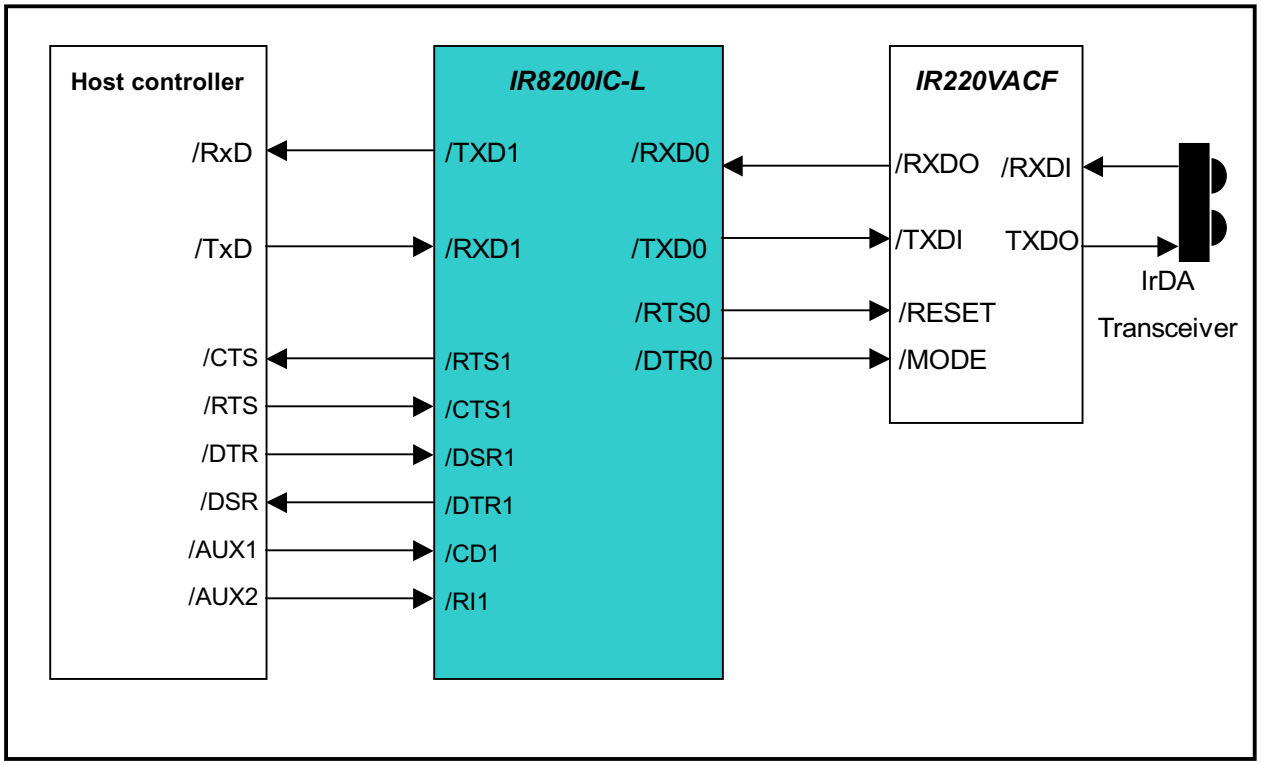
2. Overview

The ACT-IR8200IC-L is a microprocessor with on-chip IrDA protocol stack. It is designed to integrate with a “host” system. This enables the host system with IrDA communication capabilities. The host system may be a serial printer, a modem, an industrial controller, a data collector, a medical instrument, or any other device, that may benefit from being IrDA enabled.

The interface between ACT-IR8200IC-L and the host is via a traditional asynchronous serial data port.

IrDA Physical Layer (IrPHY) components are external to ACT-IR8200IC-L. This includes an IrDA encoder-decoder chip and an IrDA transceiver module.

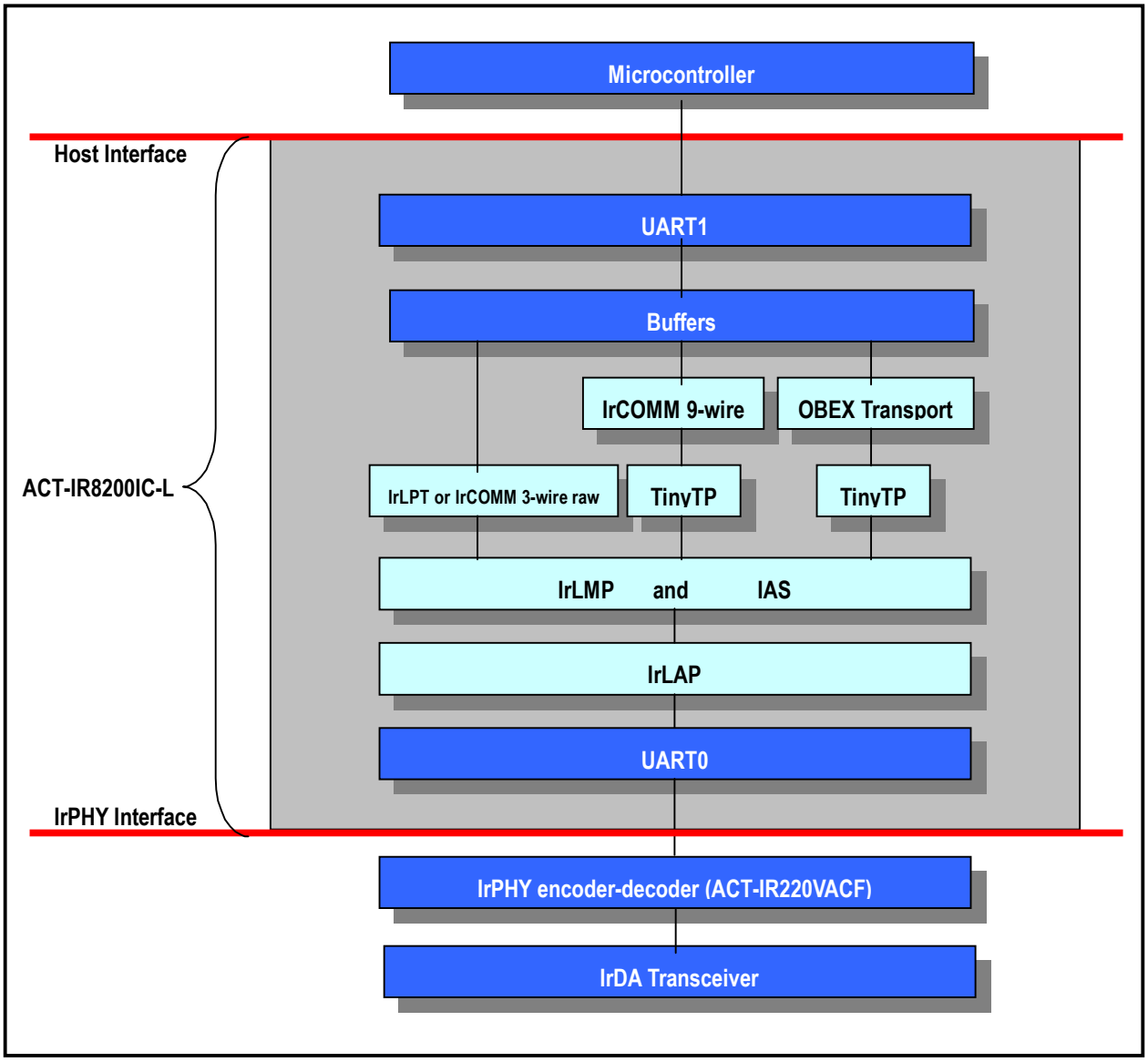
The IrPHY components and the ACT-IR8200IC-L transport data in compliance with IrDA protocol. The host system has full control of communication sessions and data flow. It needs only to handle the Application of the data transported.



3. Embedded Firmware

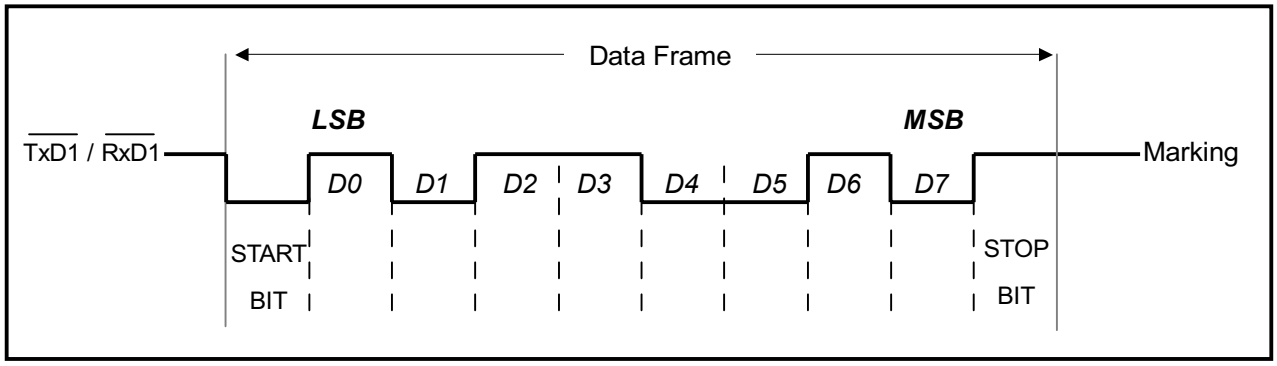
The mandatory IrDA protocol layers, IrLAP (comply with TEST frame capability requirement) and IrLMP (including IAS) are handled by ACT-IR8200IC-L, In addition, TinyTP, IrCOMM, IrLPT, IrOBEX transport are all included.

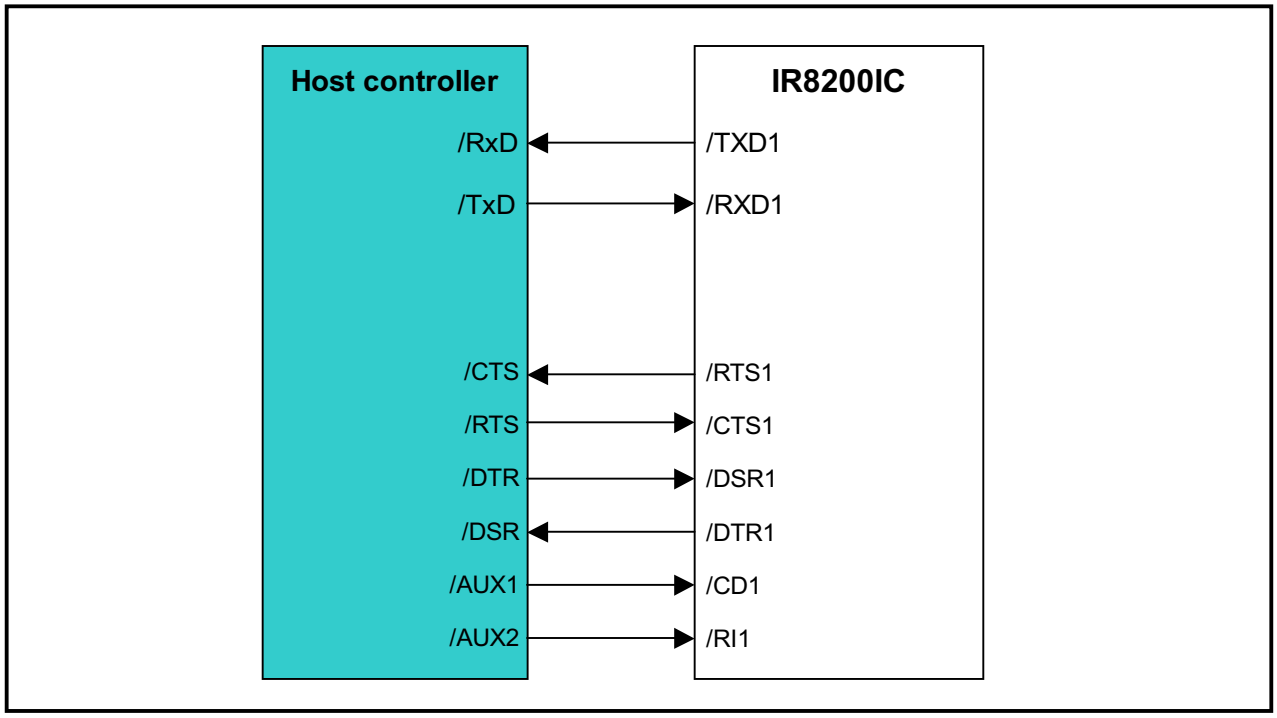
The incoming/outgoing IrDA user data payload are buffered and then transferred to/from the host. The baud rates of IrDA traffic and host interface are independent of each other. The flow controls of IrDA traffic and host interface are also independent of each other.



4. Host Interface

The host interface is a full-duplex asynchronous serial data interface. The data bytes are transmitted via /TxD1 and received via /RxD1. Each data byte consists of one start bit (0), 8 data bits (LSB first, MSB last) and a stop bit (1).





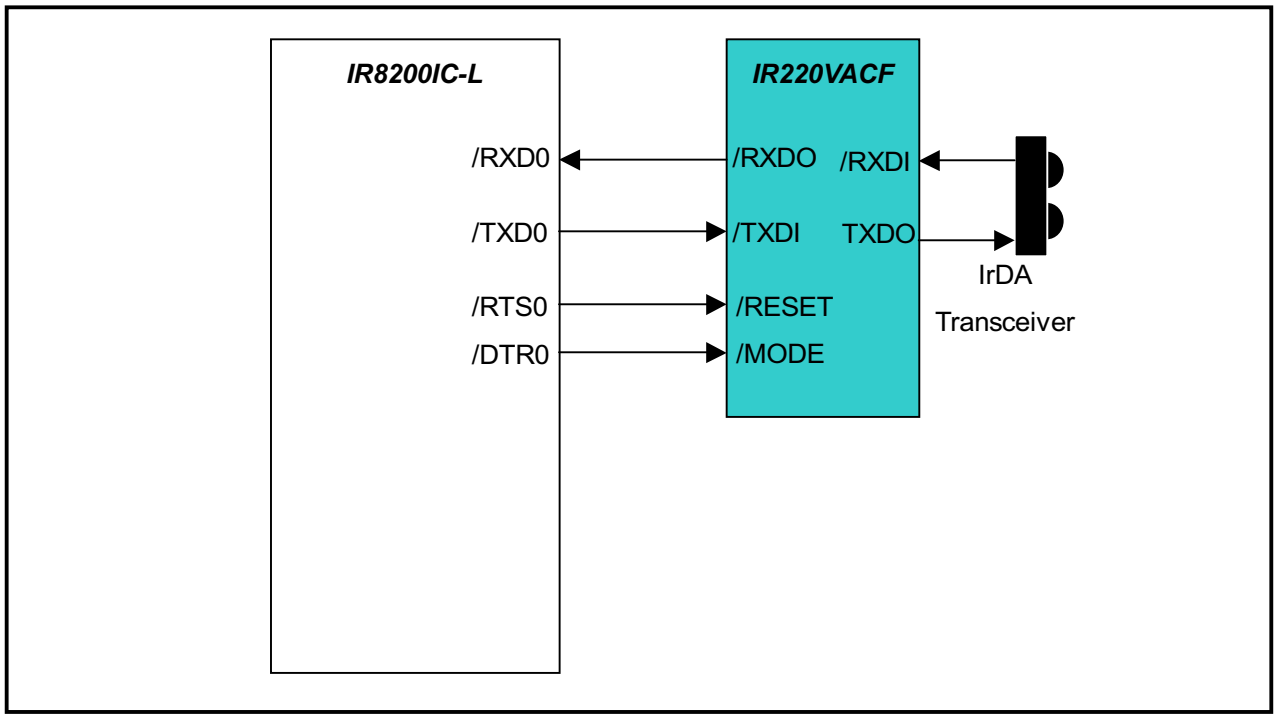
4.1 Host Interface Signals

IR8200IC-L host interface consists of three output signals and five input signals. All these signals are active low. That is, they are at 0V when active and at Vcc level when inactive. When an inverting RS232 level converter is used, the corresponding RS232 level signals are active high. That is, they are at +12V nominal when active and at –12V nominal when inactive.

1. /TxD1: serial data output.
2. /RxD1: serial data input.
3. /RTS1: output. When hardware flow control is enabled, active /RTS1 means /RxD1 is ready to receive, inactive /RTS1 means /RxD1 is not ready.
4. /CTS1: input. If hardware flow control is enabled, /CTS1 must be driven active to allow /TxD and inactive to forbid /TxD. If hardware flow control is disabled, /CTS1 is optional.
5. /DSR1: input. If connection control is enabled, /DSR1 must be driven active to allow IrDA connection and inactive to forbid a new connection or terminate an existing connection. If connection control is disabled, /DSR1 is optional.
6. /DTR1: output. If connection control is enabled, active /DTR1 means an IrDA connection is made, inactive /DTR1 means there is no connection.
7. /CD1: input. Optional.
8. /RI1: input. Optional.

5. IrPHY Interface

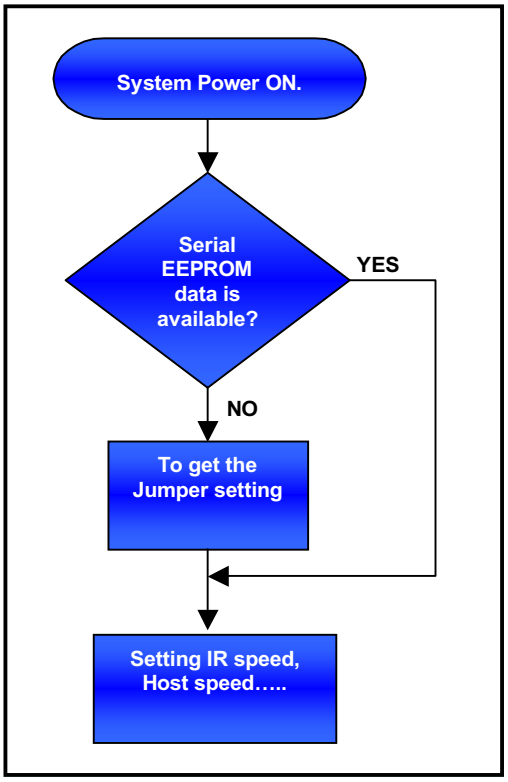
The IrPHY interface is a half-duplex asynchronous serial data interface, the data are exchanged of multiple wires (RxD, TxD) to single IR “wire” through the air.
So the IrPHY interface only working on transmitting or receiving mode, but not both at the same time.
The IrPHY interface baud rate supported: 9.6Kbps, 19.2kbps, 38.4kbps, 57.6kbps, 115.2kbps.



6. Jumpers and other optional hardware

6.1 Interfacing Serial EEPROM with IR8200IC-L

There are some special functions if the external serial EEPROM installed.
The optional serial EEPROM allow users to set ”Host Speed” and “Hardware Flow Control and Connection Control”. The system initial sequence are shown below:



Note: The serial EEPROM setting can override jumper settings.

6.2 Baud Rate Setting

Jumpers SEL0-2 and serial EPROM settings are used to set the host interface /RxD1 and /TxD1 data rate. Note that this is independent of the IrDA connection data rate.
Data format is always 8 data bits, no parity, and 1 stop bit. Note that this is compatible with end-to-end data format using 7 data bits, parity, and 1 stop bit. That is, the application at both end of the IrDA link may generate and check parity if 7 data bit is used.
The Host Interface can operate on eight different baud rates from 1.2kbps to 115.2kbps.

Baud Rate	Jumpers		
	SEL2	SEL1	SEL0
1.2kbps	0	0	0
2.4kbps	0	0	1
4.8kbps	0	1	0
9.6kbps	0	1	1
19.2kbps	1	0	0
38.4kbps	1	0	1
57.6kbps	1	1	0
115.2kbps	1	1	1

6.3 Hardware Flow Control and Connection Control

Jumper SEL3 and serial EEPROM settings are used to enable or disable host interface hardware flow control and connection control.

If this function enabled, the host must drive /DSR1 and /CTS1.

1. /RTS1 is used to for flow control of /RxD1. Active /RTS1 permits /RxD1. Inactive /RTS1 forbids /RxD1.
2. /CTS1 is used for flow control of /TxD1. Active /CTS1 permits /TxD1. Inactive /CTS1 forbids /TxD1.
3. /DSR1 is used for connection control. Active /DSR1 permits IrDA connection. Inactive /DSR1 forbids new connection and terminates existing connection.
4. /DTR1 is used to indicate if IrDA connection is active or not.

If this function disable, no hardware flow control used.

1. Output /DTR1 and /RTS1 according to IrLMP DTE Line Settings and Changes parameter.
2. If IrCOMM 9-wire is connected and host DCE Line states is changed (which is the /CTS1, /DSR1, /RI1, /CD1), IR8200IC-L will response a DCE Line Settings and Changes parameter via IrLMP control channel.

Function	Jumper SEL3	Descriptions
Disable	0	Disable Hardware Flow Control and Connection Control
Enable	1	Enable Hardware Flow Control and Connection Control

Independent of the jumper or serial EEPROM settings, software flow control is automatically used and /DTR1 always active during IrLPT connection (this is used for printer host). In this case, if /RxD1 received an X-OFF, /TxD1 transmission is blocked. If /RxD1 received an X-ON, /TxD1 transmission may resume. In addition, hardware flow control may also be enable.

6.4 IrCOMM Modem Status, Modem Control, etc.

IrDA IrCOMM 9-wire protocol allows the Primary to read or pull the Secondary modem status lines (/DSR1, /CTS1, /CD1, and /RI1 input signals). IR8200IC-L always comply with this specification. IrCOMM 9-wire also allows the Primary to control the Secondary modem control lines (/DTR1 and /RTS1 output signals). IR8200IC-L complies with this specification only when hardware flow control and connection control are disabled. When hardware flow control and connection control are enabled, these output signals do not obey the Primary.
IrCOMM 9-wire further allows the Primary to control the Secondary data rate, data format, flow control, and /TxD break. IR8200IC-L does not obey these commands from the Primary.

6.5 Evaluation and Reference Design

It is recommended that you verify the compatibility with your host system by using our IrDA Protocol to RS232 Adapter, IR100S-L. This is a self-content unit, with IR8200IC-L, IrPHY components, RS232-level converters and external AC power source, all built into a compact package. Also available for quick IrDA implementation is the internal PCB version, IR100S-L which enables your host system to be IrDA (IrReady) certifiable immediately.

IR100S-L is designed to enable instant IrDA capability of your host via RS232 serial port; e.g. modem, serial printer, instrumentation, meter, data terminal, medical device. Once IR100S-L is proven to work well with your host system, and upon execution of mutual NDA and purchasing terms, we'll provide circuit diagrams to help speed up your implementation.

7. Packages:

- PLCC 44
- QFP 44

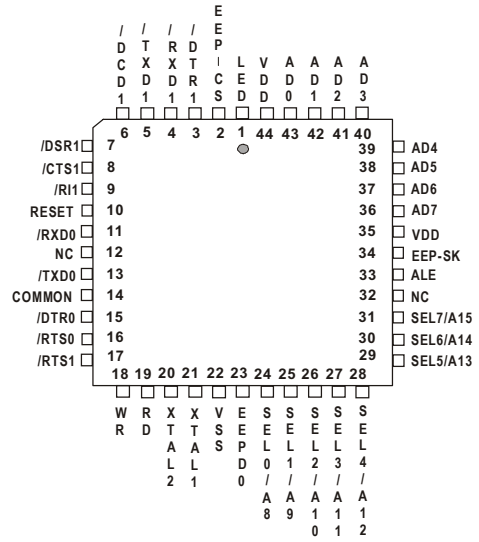
DC electrical characteristics:
- Operating voltage: 2.7 ~ 5.5 VDC
- Operating current: Active<50mA (No load)

Operating temperature:
- 0°C ~ +70°C
- -40°C ~ +85°C (Industrial Temperature version).

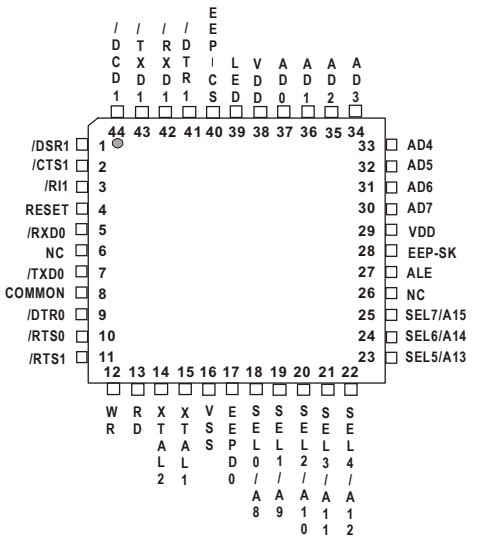
Storage temperature:
- -55°C ~ +150°C

8. PIN Configuration

44-Pin PLCC



44-Pin QFP



9. PIN Description

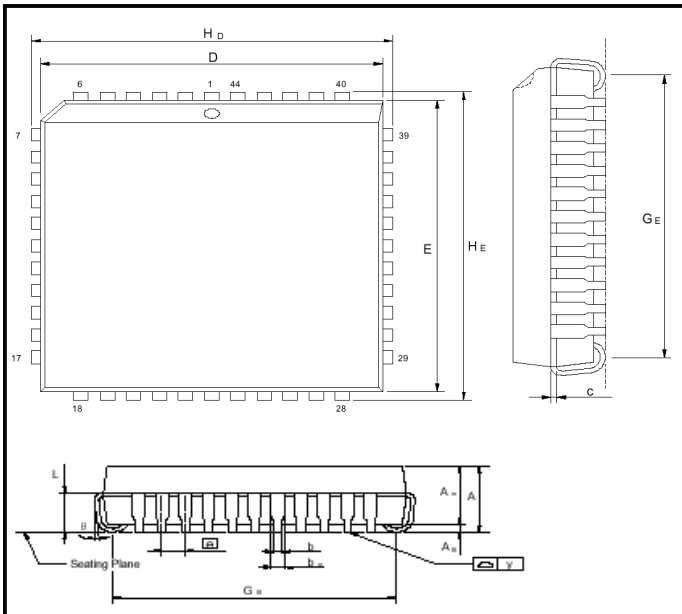
Group	Symbol	Pin No. (PLCC)	Pin No. (QFP)	I/O Type	Descriptions
1	/DTR1	3	41	O	Data terminal Readv
	/RXD1	4	42	I	Receiver Data from Host
	/TXD1	5	43	O	Transmitter Data to Host
	/CD1	6	44	I	Data Carrier Detect
	/DSR1	7	1	I	Data Set Ready
	/CTS1	8	2	I	Clear To Send
	/RI1	9	3	I	Ring Indicator
	/RTS1	17	11	O	Request To Send
2	EEP-SK	34	28	I/O	EEPROM clock
	EEP-DO	23	17	I/O	EEPROM data
	EEP-CS	2	40	O	EEPROM Chip Select
	A7 ~ A0	36 ~ 43	30 ~ 37	I/O	External RAM address bus
	D7 ~ D0	36 ~ 43	30 ~ 37	I/O	External RAM data bus
	A8 ~ A15	24 ~ 31	18 ~ 25	O	External RAM address bus
	ALE	33	27	O	Address latch enable
3	SEL0	24	18	I	Host baud rate selection
	SEL1	25	19		
	SEL2	26	20		
	SEL3	27	21		Flow control and connection control SEL.
	SEL4 ~ SEL7	28 ~ 31	22 ~ 25		Reserved for future use
	COMMON	14	8	O	Common return for SEL0 ~ SEL6
4	/RTS0	16	10	O	ACT-IR220VACF reset signal
	/DTR0	15	9	O	ACT-IR220VACF mode selection
	/TXD0	13	7	O	Data out to ACT-IR220VACF
	/RXD0	11	5	I	Data in from ACT-IR220VACF
5	LED	1	39	O	Svstem status indicator
	VDD	44	38	-	Supply voltage for operation
	VSS	22	16	-	Ground potential
	XTAL1	21	15	I	Crystal oscillator input
	XTAL2	20	14	O	Crystal oscillator output
	RESET	10	4	I	Reset the device

TYPE **I**: Input, **O**: Output

GROUP **1**: Host Interface, **2**: Optional hardware, **3**: Jumper setting, **4**: IrPHY Interface, **5**: Others

10. Package Dimensions

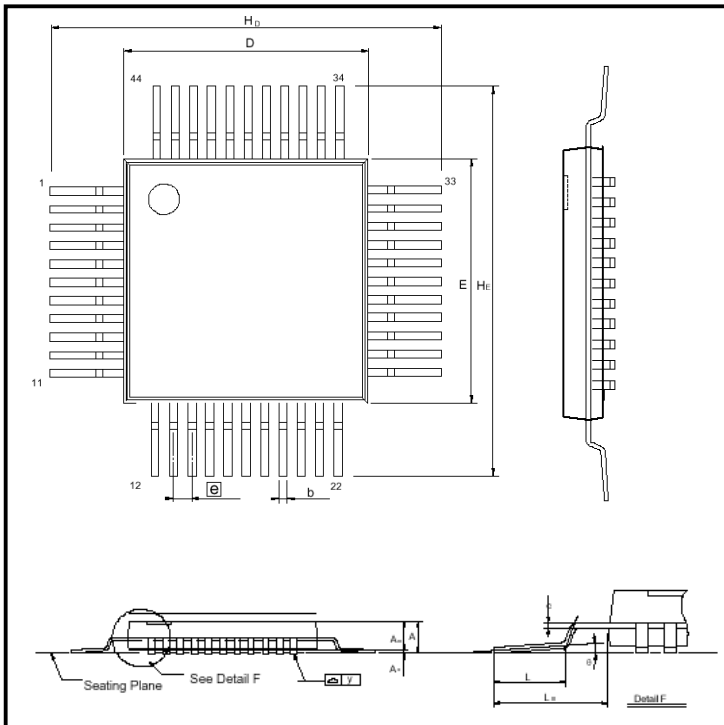
44-PIN PLCC



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.185	—	—	4.699
A_1	0.020	—	—	0.508	—	—
A_2	0.145	0.150	0.155	3.683	3.81	3.937
b_1	0.026	0.028	0.032	0.66	0.711	0.813
b	0.016	0.018	0.022	0.406	0.457	0.559
c	0.008	0.010	0.014	0.203	0.254	0.356
D	0.648	0.653	0.658	16.46	16.59	16.71
E	0.648	0.653	0.658	16.46	16.59	16.71
e	0.050 BSC			1.27 BSC		
G_D	0.590	0.610	0.630	14.99	15.49	16.00
G_E	0.590	0.610	0.630	14.99	15.49	16.00
H_D	0.680	0.690	0.700	17.27	17.53	17.78
H_E	0.680	0.690	0.700	17.27	17.53	17.78
L	0.090	0.100	0.110	2.296	2.54	2.794
y	—	—	0.004	—	—	0.10

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Controlling dimension: Inches
4. General appearance spec. should be based on final visual inspection spec.

44-PIN QFP



Symbol	Dimension in inch			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	---	---	---	---	---	---
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	0.025	0.031	0.036	0.635	0.80	0.952
H_D	0.510	0.520	0.530	12.95	13.2	13.45
H_E	0.510	0.520	0.530	12.95	13.2	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	0.051	0.063	0.075	1.295	1.6	1.905
y	—	—	0.003	—	—	0.08
θ	0°	—	7°	0°	—	7°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. should be based on final visual inspection spec.